

TOSHIBA Field Effect Transistor Silicon N Channel MOS Type ( $\pi$ -MOS $\pi$ )

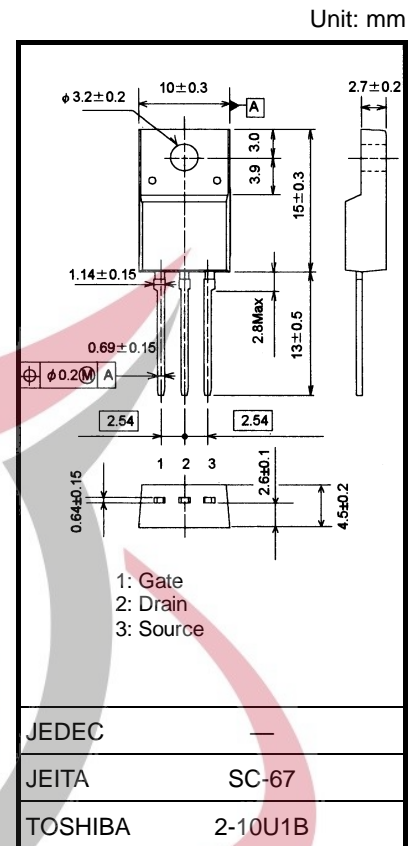
# TK8A50D

## Switching Regulator Applications

- Low drain-source ON-resistance:  $R_{DS(ON)} = 0.7 \Omega$  (typ.)
- High forward transfer admittance:  $|Y_{fs}| = 4.0 S$  (typ.)
- Low leakage current:  $I_{DSS} = 10 \mu A$  (max) ( $V_{DS} = 500 V$ )
- Enhancement mode:  $V_{th} = 2.0$  to  $4.0 V$  ( $V_{DS} = 10 V, I_D = 1 mA$ )

## Absolute Maximum Ratings ( $T_a = 25^\circ C$ )

Characteristics		Symbol	Rating	Unit
Drain-source voltage		$V_{DSS}$	500	V
Gate-source voltage		$V_{GSS}$	$\pm 30$	V
Drain current	DC (Note 1)	$I_D$	8	A
	Pulse ( $t = 1 ms$ ) (Note 1)	$I_{DP}$	32	
Drain power dissipation ( $T_c = 25^\circ C$ )		$P_D$	40	W
Single pulse avalanche energy (Note 2)		$E_{AS}$	165	mJ
Avalanche current		$I_{AR}$	8	A
Repetitive avalanche energy (Note 3)		$E_{AR}$	4.0	mJ
Channel temperature		$T_{ch}$	150	$^\circ C$
Storage temperature range		$T_{stg}$	-55 to 150	$^\circ C$



Weight : 1.7 g (typ.)

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings. Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

## Thermal Characteristics

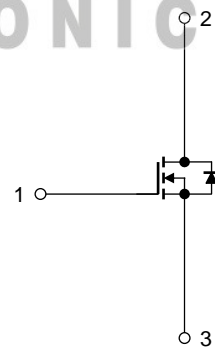
Characteristics	Symbol	Max	Unit
Thermal resistance, channel to case	$R_{th(ch-c)}$	3.125	$^\circ C/W$
Thermal resistance, channel to ambient	$R_{th(ch-a)}$	62.5	$^\circ C/W$

Note 1: Ensure that the channel temperature does not exceed  $150^\circ C$ .

Note 2:  $V_{DD} = 90 V, T_{ch} = 25^\circ C$  (initial),  $L = 4.4 mH, R_G = 25 \Omega, I_{AR} = 8 A$

Note 3: Repetitive rating: pulse width limited by maximum channel temperature

This transistor is an electrostatic-sensitive device. Handle with care.



Start of commercial production  
2008-07

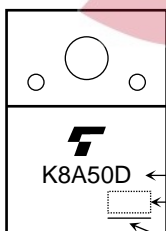
**Electrical Characteristics (Ta = 25°C)**

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current	$I_{GSS}$	$V_{GS} = \pm 30\text{ V}, V_{DS} = 0\text{ V}$	—	—	$\pm 1$	$\mu\text{A}$
Drain cut-off current	$I_{DSS}$	$V_{DS} = 500\text{ V}, V_{GS} = 0\text{ V}$	—	—	10	$\mu\text{A}$
Drain-source breakdown voltage	$V_{(BR)DSS}$	$I_D = 10\text{ mA}, V_{GS} = 0\text{ V}$	500	—	—	V
Gate threshold voltage	$V_{th}$	$V_{DS} = 10\text{ V}, I_D = 1\text{ mA}$	2.0	—	4.0	V
Drain-source ON-resistance	$R_{DS(ON)}$	$V_{GS} = 10\text{ V}, I_D = 4\text{ A}$	—	0.7	0.85	$\Omega$
Forward transfer admittance	$ Y_{fs} $	$V_{DS} = 10\text{ V}, I_D = 4\text{ A}$	1.0	4.0	—	S
Input capacitance	$C_{iss}$	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	—	800	—	pF
Reverse transfer capacitance	$C_{rss}$		—	4	—	
Output capacitance	$C_{oss}$		—	100	—	
Switching time	Rise time	$t_r$		—	20	ns
	Turn-on time	$t_{on}$		—	40	
	Fall time	$t_f$		—	12	
	Turn-off time	$t_{off}$		—	60	
Total gate charge	$Q_g$	$V_{DD} \approx 400\text{ V}, V_{GS} = 10\text{ V}, I_D = 8\text{ A}$	—	16	—	nC
Gate-source charge	$Q_{gs}$		—	10	—	
Gate-drain charge	$Q_{gd}$		—	6	—	

**Source-Drain Ratings and Characteristics (Ta = 25°C)**

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Continuous drain reverse current (Note 1)	$I_{DR}$	—	—	—	8	A
Pulse drain reverse current (Note 1)	$I_{DRP}$	—	—	—	32	A
Forward voltage (diode)	$V_{DSF}$	$I_{DR} = 8\text{ A}, V_{GS} = 0\text{ V}$	—	—	-1.7	V
Reverse recovery time	$t_{rr}$	$I_{DR} = 8\text{ A}, V_{GS} = 0\text{ V},$	—	1200	—	ns
Reverse recovery charge	$Q_{rr}$	$dI_{DR}/dt = 100\text{ A}/\mu\text{s}$	—	10	—	$\mu\text{C}$

**Marking**



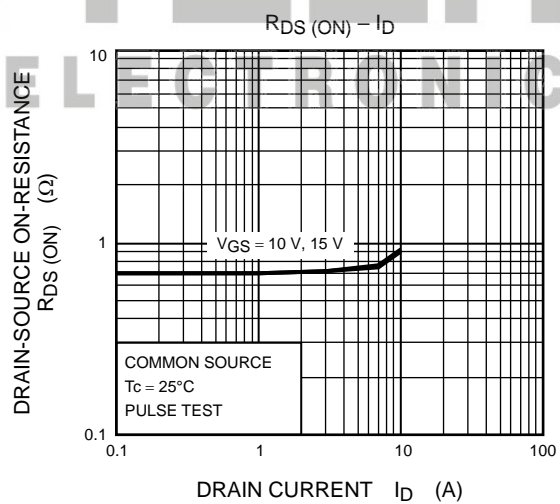
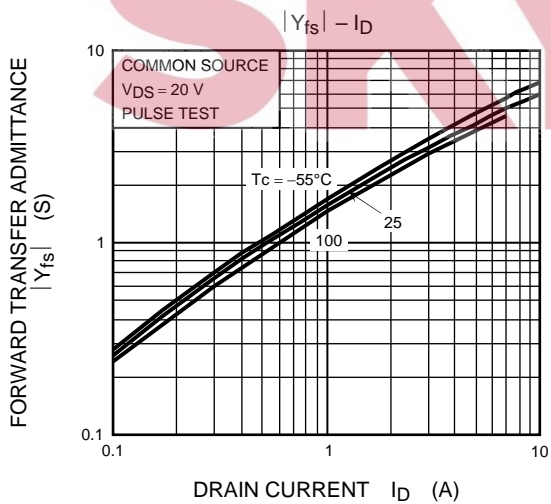
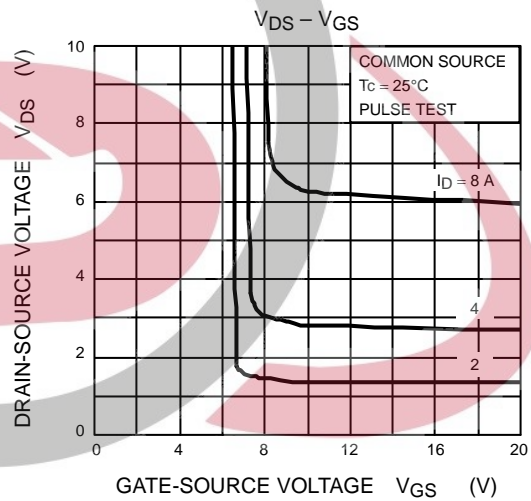
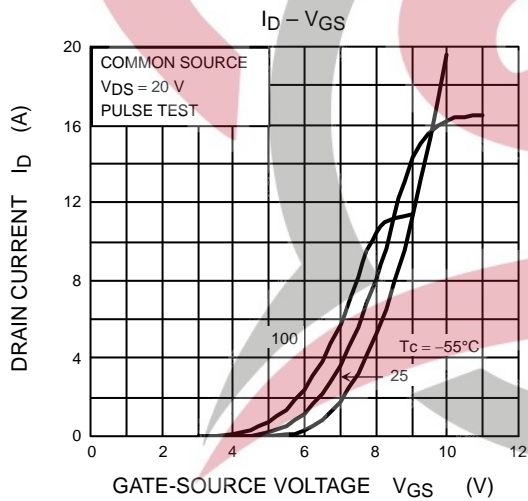
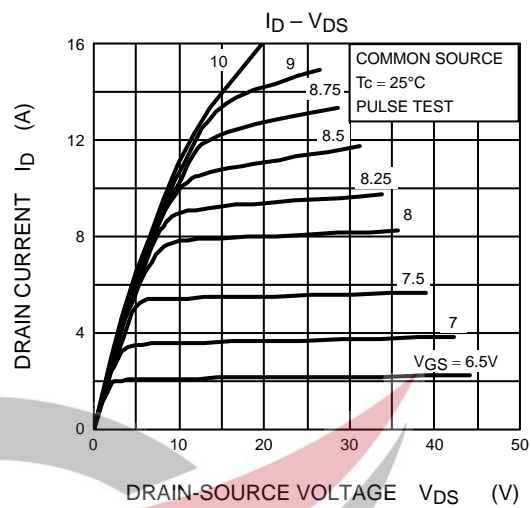
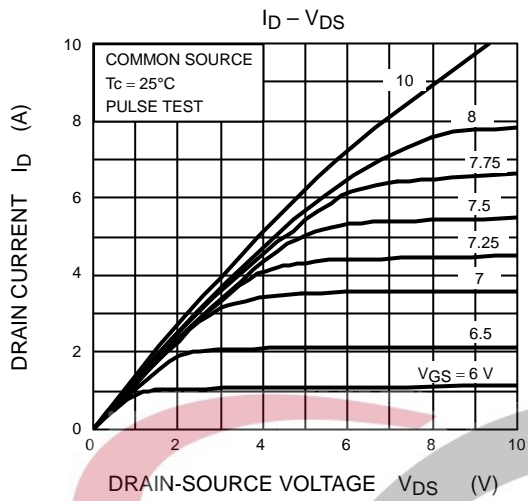
Part No. (or abbreviation code)  
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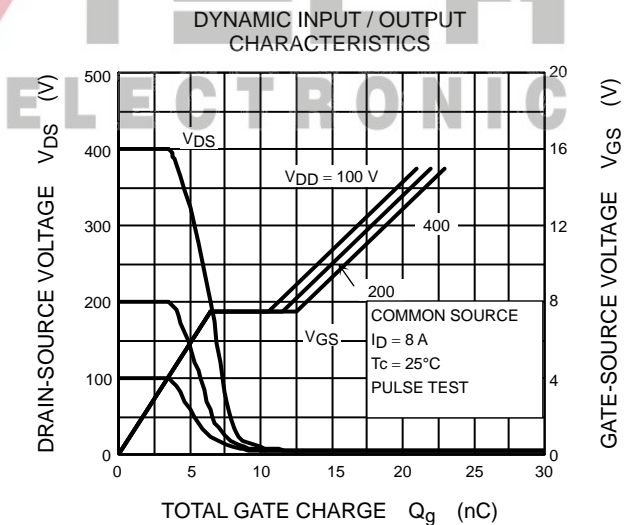
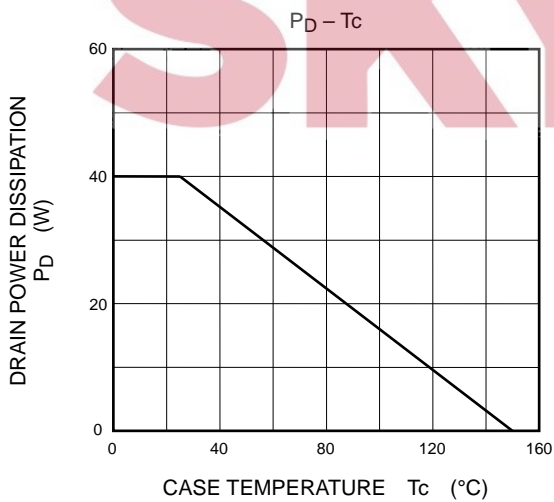
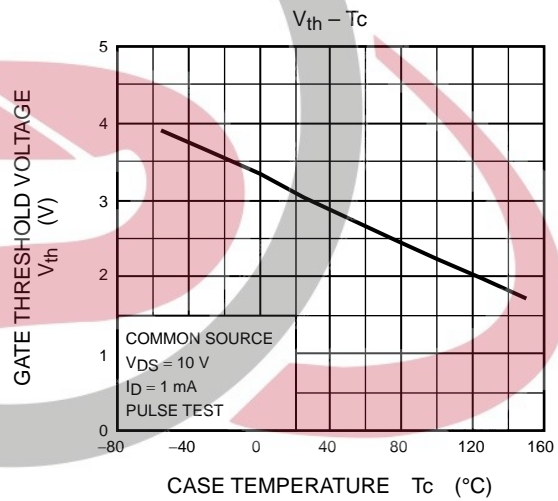
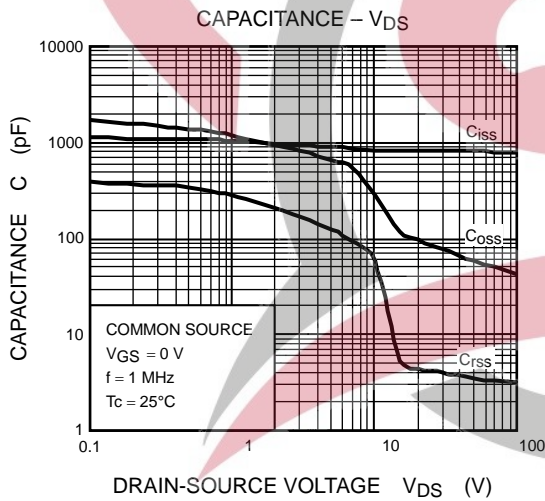
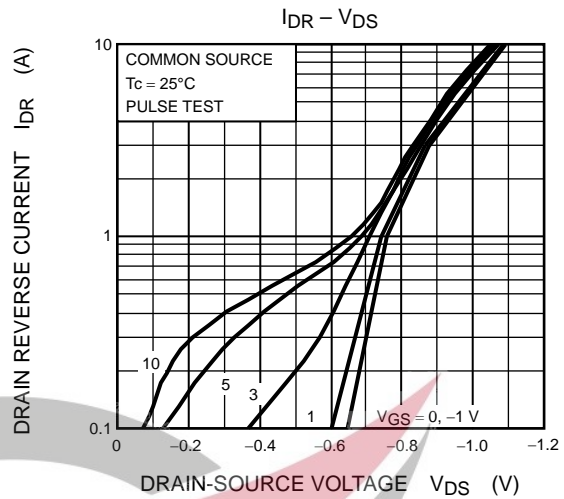
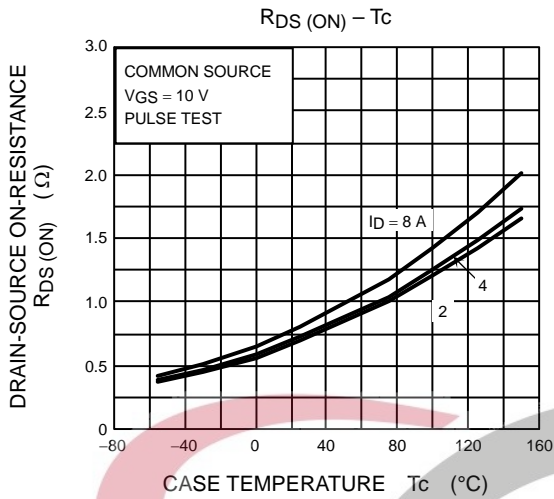
Note 4

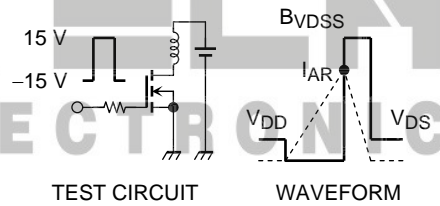
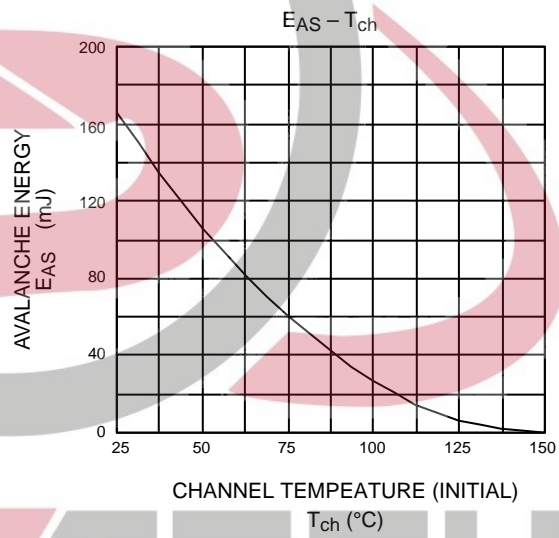
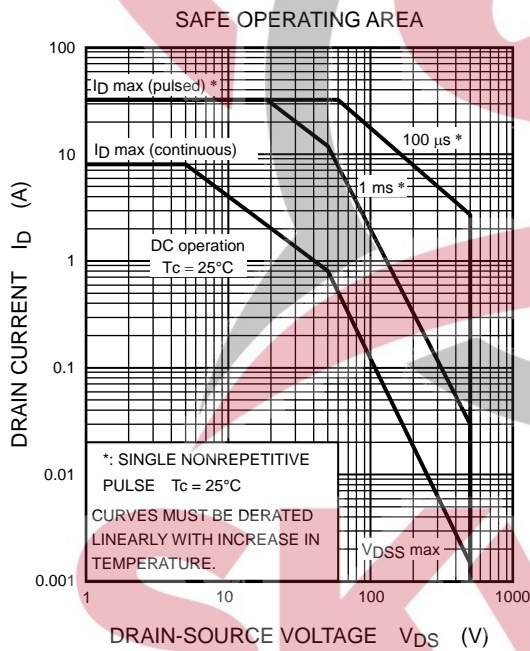
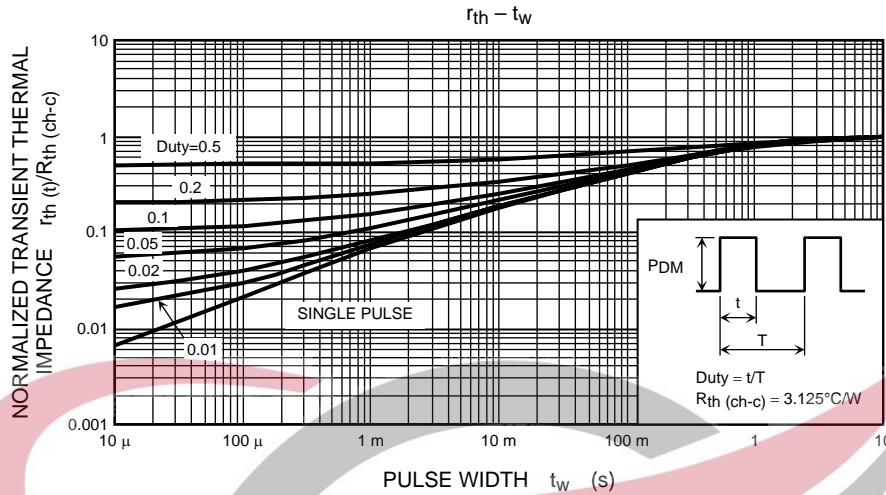
Note 4: A line under a Lot No. identifies the indication of product Labels.

[[G]]/RoHS COMPATIBLE or [[G]]/RoHS [[Pb]]

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$$E_{AS} = \frac{1}{2} \cdot L \cdot I^2 \cdot \left( \frac{B_{VDSS}}{B_{VDSS} - V_{DD}} \right)$$

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